KEIL SIMULATOR WITH BLDC EXAMPLE FOR XC866

October 2005

Industrial and Multimarket Microcontroller

Infineon technologies

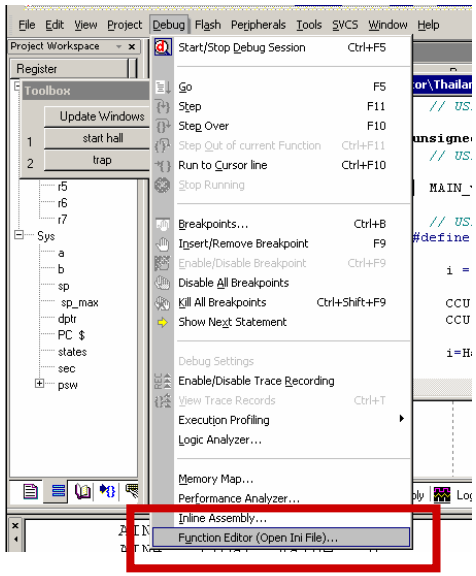
Never stop thinking.

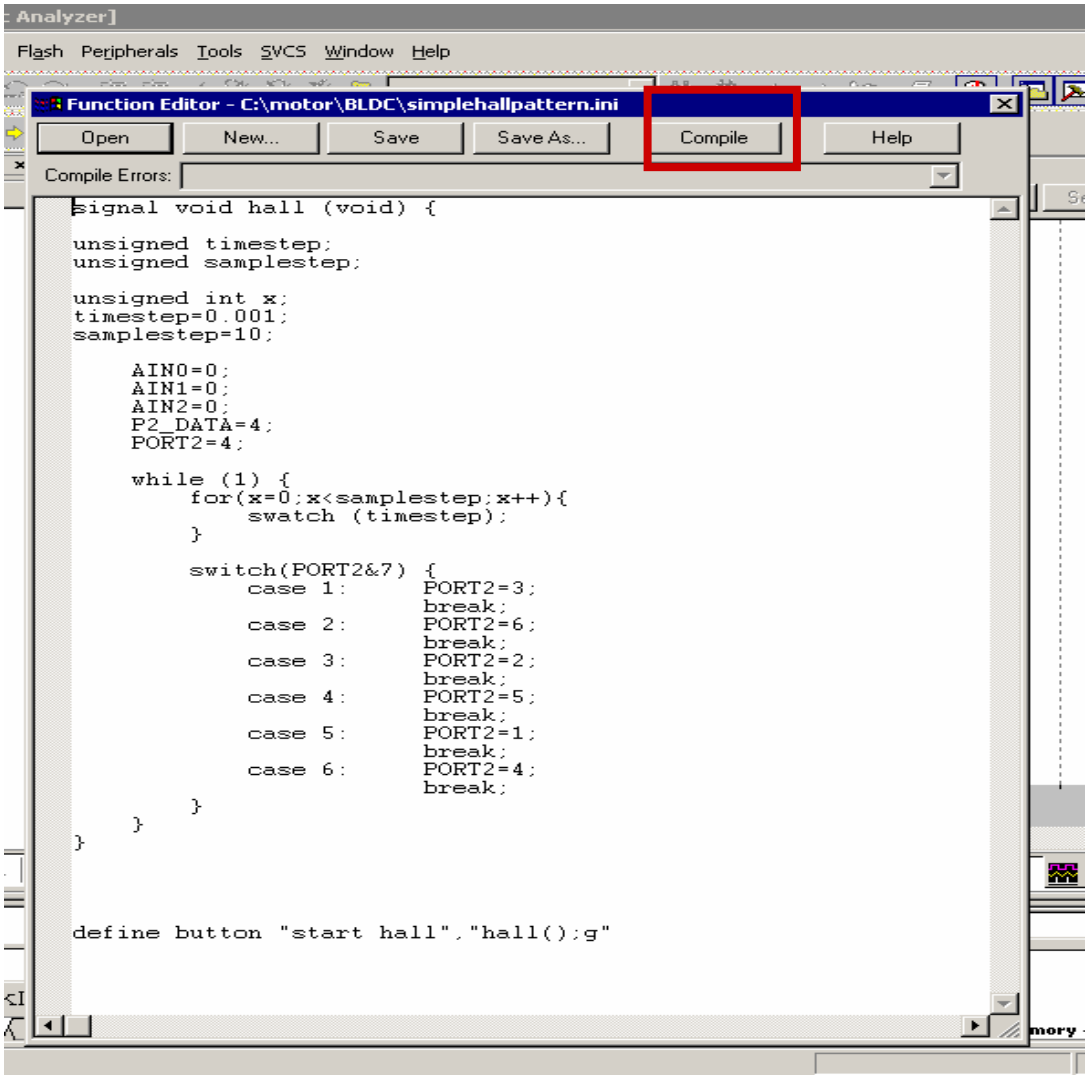
Why Simulator

- Designing certain system is safer if the code can be verified first in simulation. Bugs in the code can stress the system - burn the board!!
- The configurations of the peripherals of XC866 are best checked in simulation and fine tuned before trying on the setup.
- With the KEIL logic analyzer providing the interface, you have a graphical learning tool that is fast and easy to use.

Simple stimuli for Simulator

- Script is in C
- Hall pattern generator
- Buttons to run the simulation
- Output with simple BEMF
- An example hallpattern.ini is included.





Anatomy of a simple stimuli script for Simulator

- Refer to hallpattern.ini included in the hands on.
- 'Signal' function are for outputting to the logic analyzer.
- Swatch() programs period between state changes, the argument is in seconds.
- It can call other functions. The auxillary functions are declared with 'func'
- Create buttons to run the 'signal' functions.

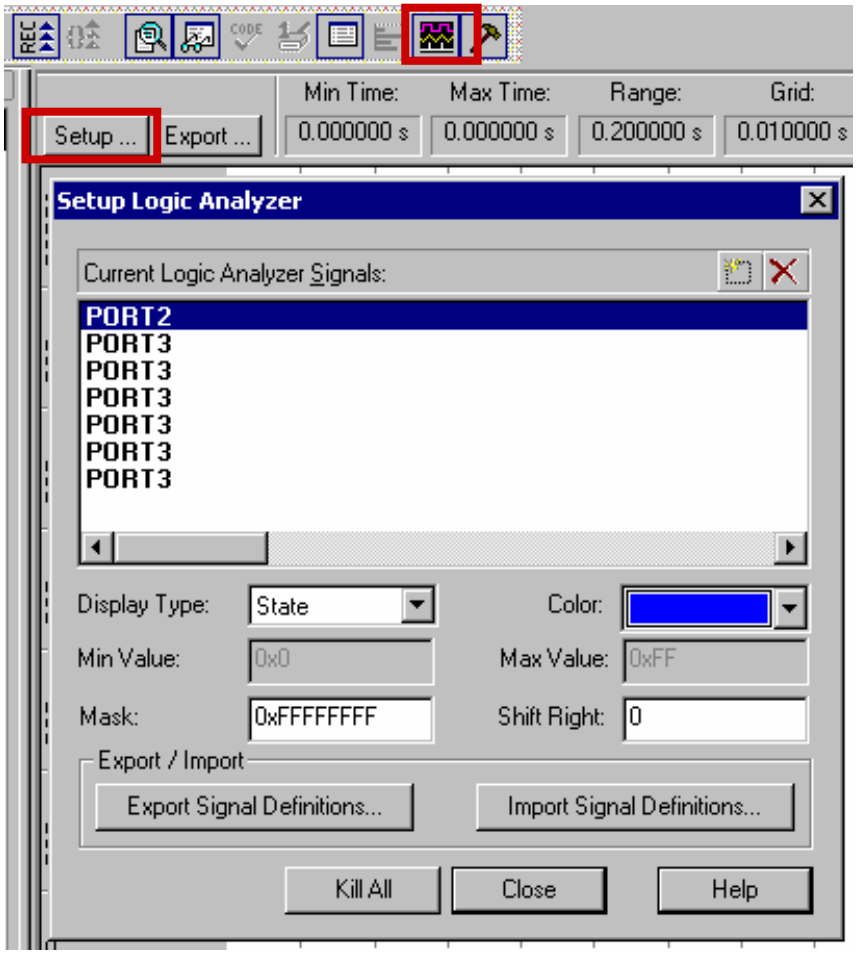
```
signal void hall (void) {
unsigned int temp;
float v;
unsigned samplestep;
unsigned int x;
unsigned char direction,hallstate;
samplestep=10;


    AIN4=0;
    AIN5=0;
    AIN6=0;
    P2_DATA=5;
    PORT2=5;
    PORT3|=0x40;
    swatch(0.15)

    while (1) {
        hallstate=PORT2&7;
        for(x=0;x<samplestep;x++){
            swatch (0.001);
            direction = sensorless(samplestep,hallstate);
        }
        switch(PORT2&7) {
            case 1:      if(direction==0)PORT2=5;
```

```
func unsigned char sensorless (float step, unsigned char hallstate){
unsigned char direction;
//direction 0 is forward
switch( MCMOUTL )
    {
    case 0x23:      AIN5=0;
                    AIN6=5;
```

```
define button "start hall","hall();g"
define button "trap", "trap()"
```

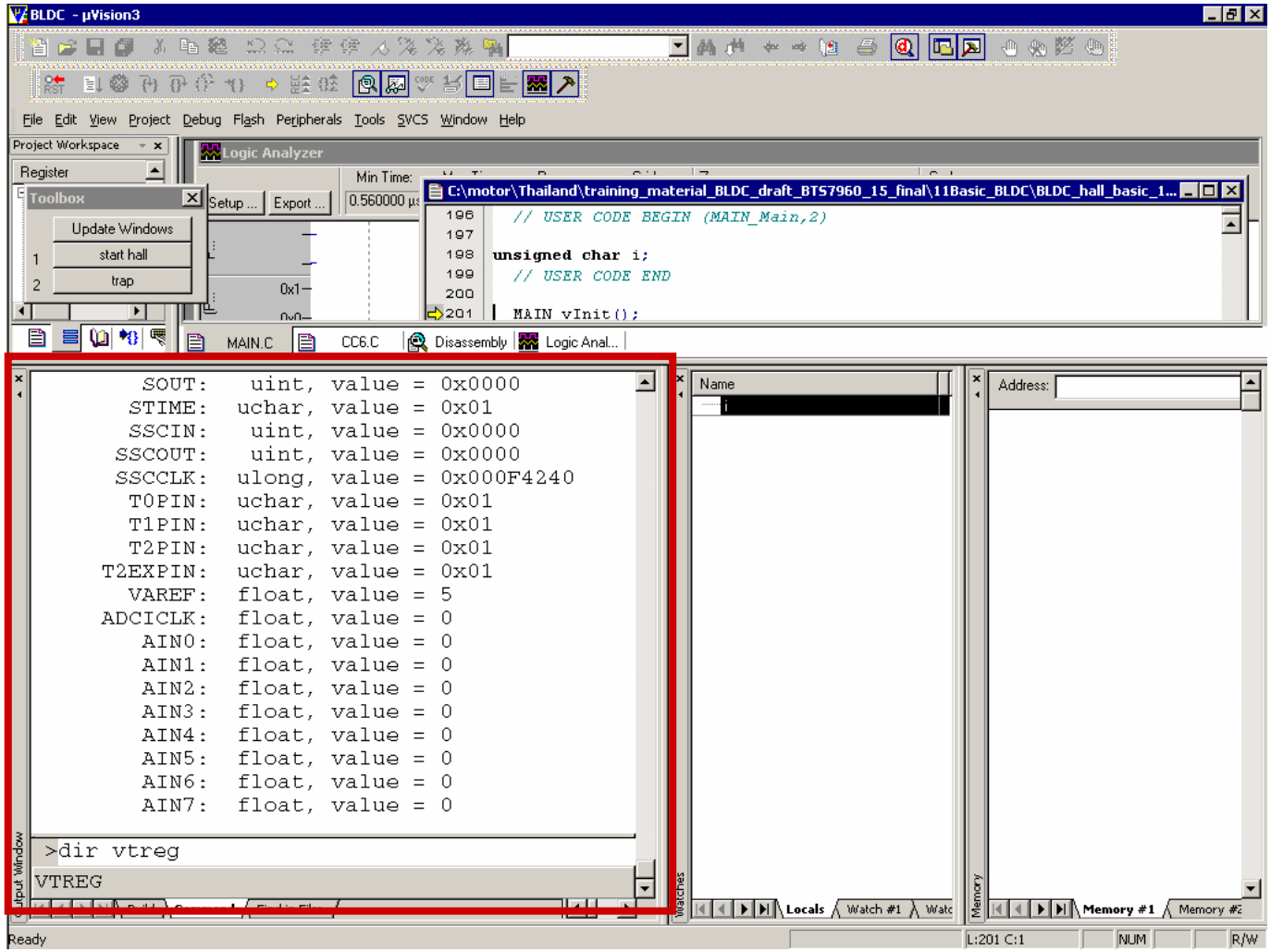
Select signals to be displayed on the Logic Analyzer

- Select Port 2 to be displayed the hall signals in the state format.
- Select Port 3 pins to be displayed in bit format. (Key in PORT3.x for pin 3.x)
- An example, hallpattern.uvl, is included



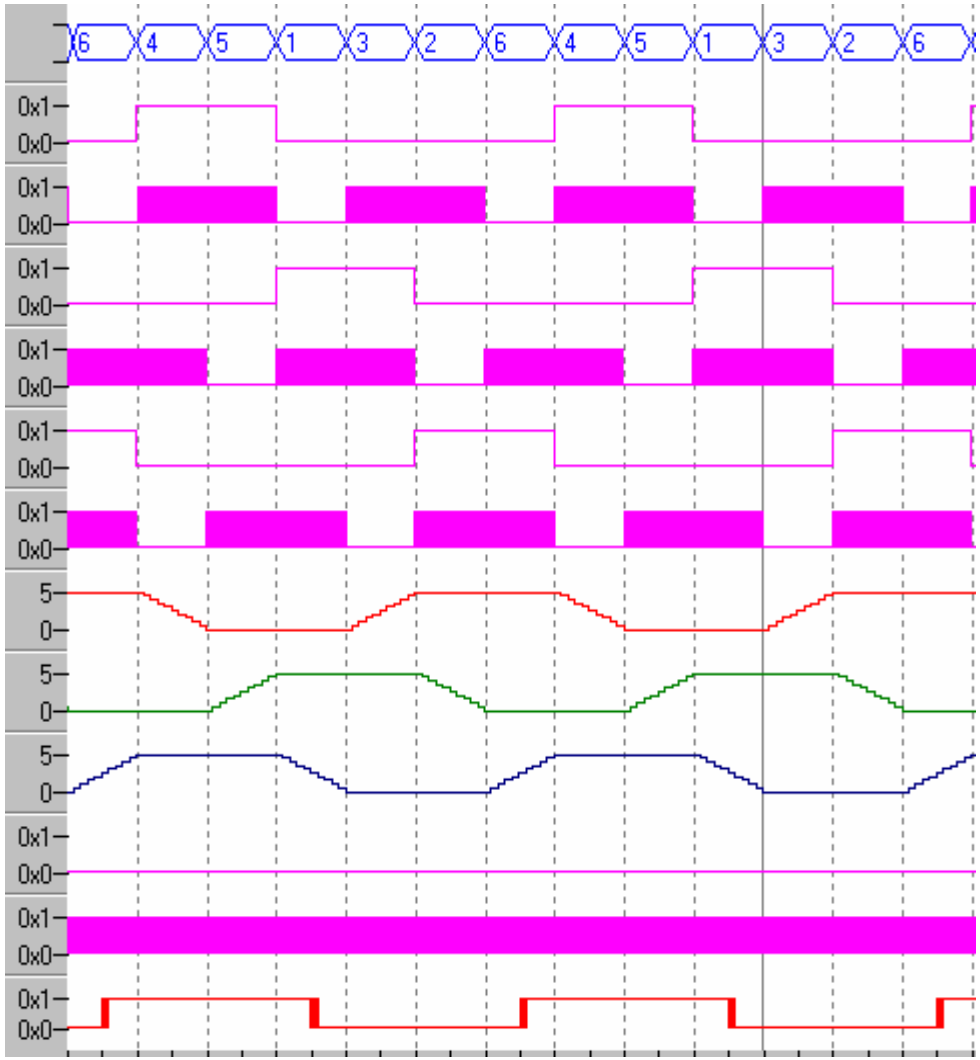
Select signals to be displayed on the Logic Analyzer

- For a default list of available signals, type in 'DIR VTREG' in the output window. The list will be shown.
- User defined signals by using free tools available from Keil.

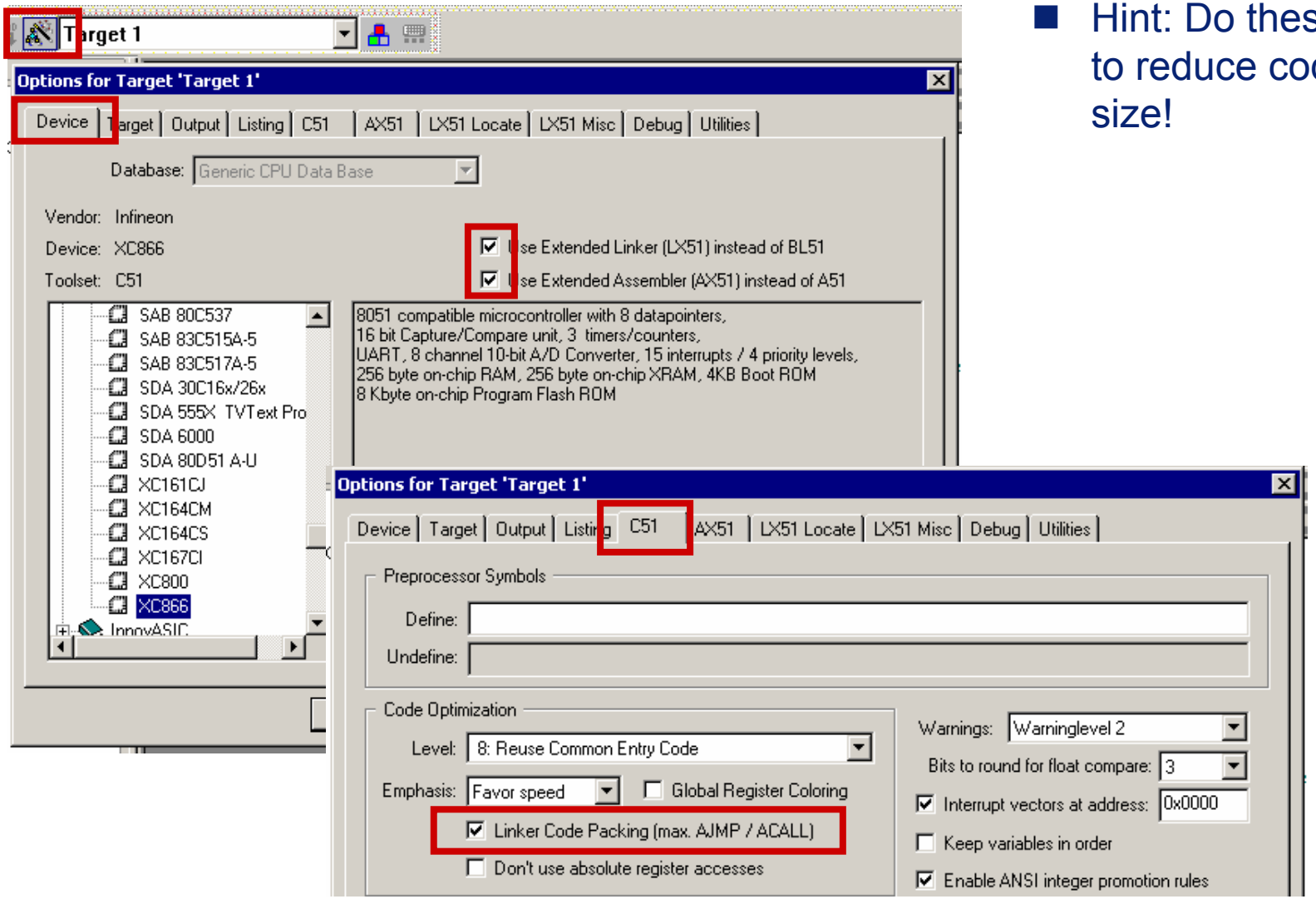


Logic Analyzer signal definition with hallpattern.uvl

- Hall pattern
- CC60
- COUT60
- CC61
- COUT61
- CC62
- COUT62
- A
- B
- C
- TRAP
- COUT63
- PORT0.2

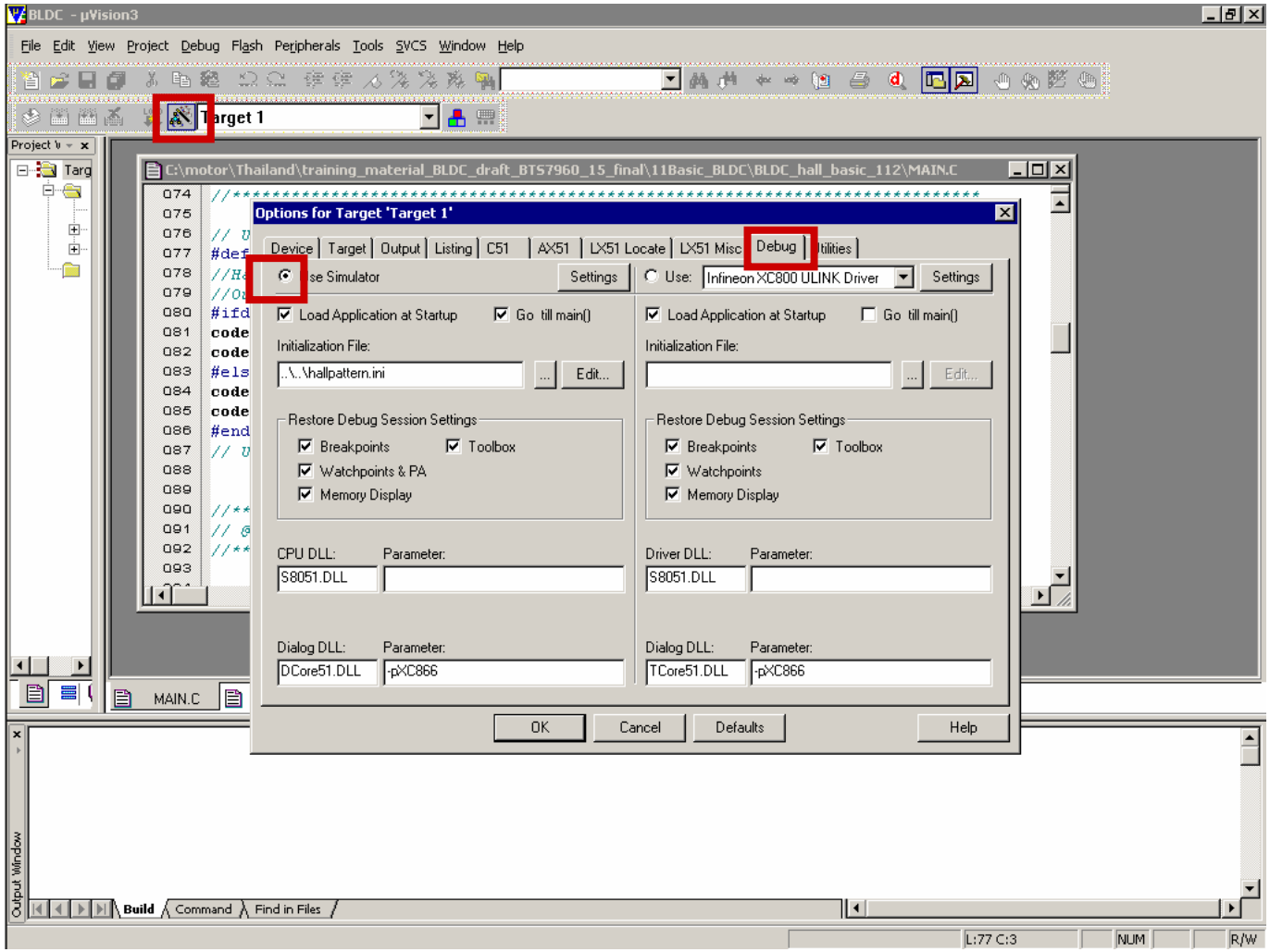


Compile and run Debug session with Logic Analyzer



- Hint: Do these to reduce code size!

Compile and run Debug session with Logic Analyzer



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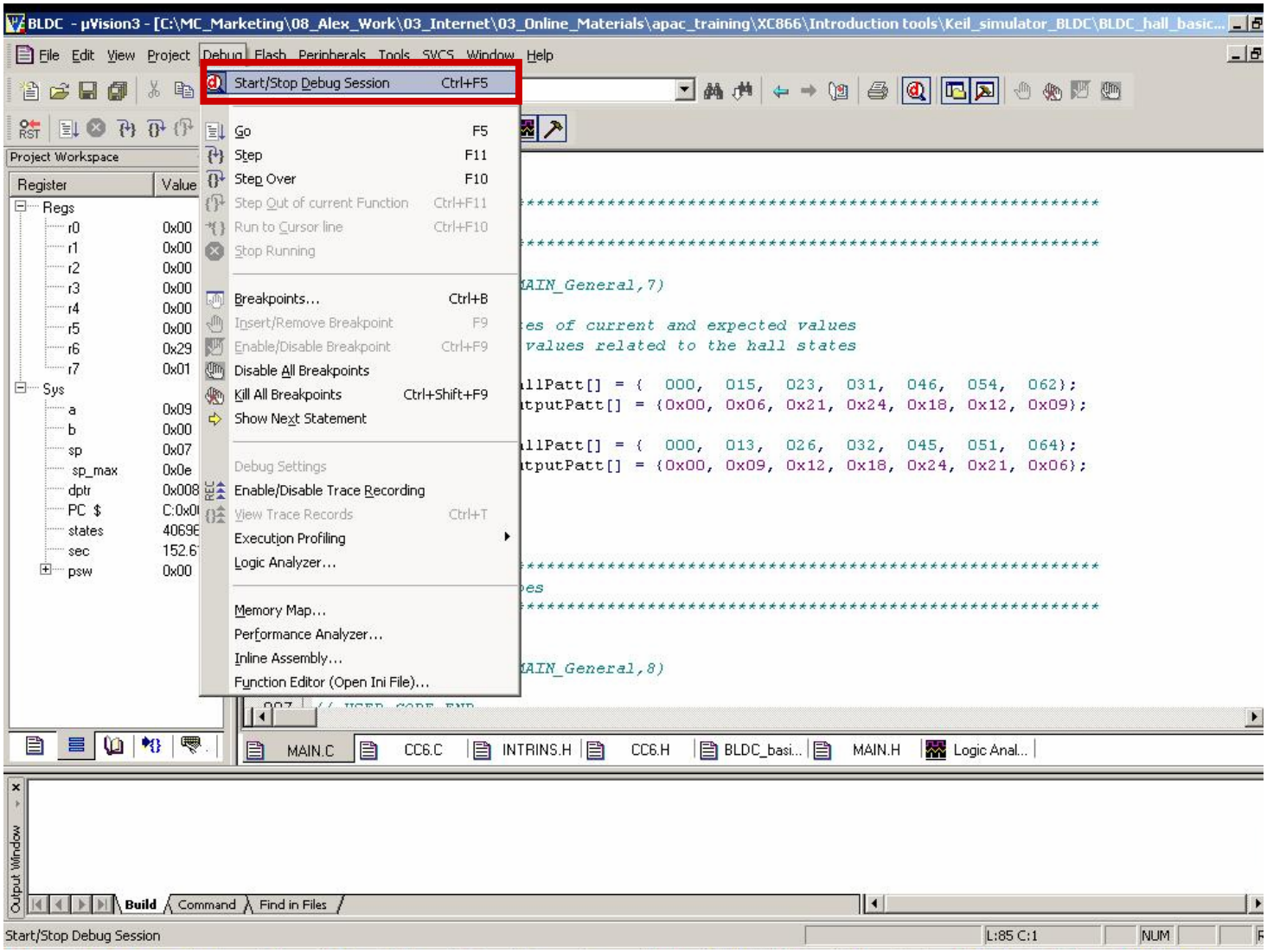

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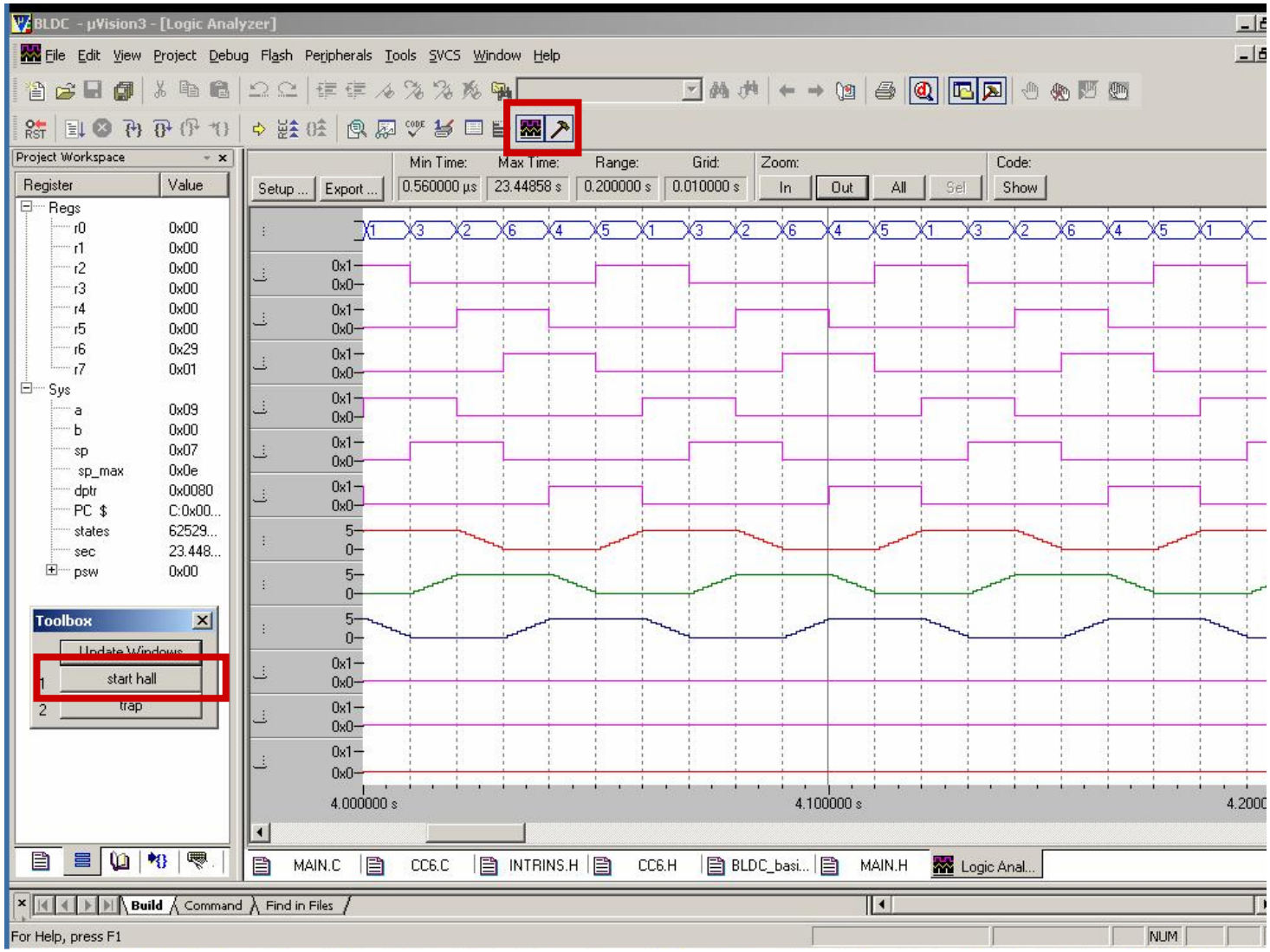
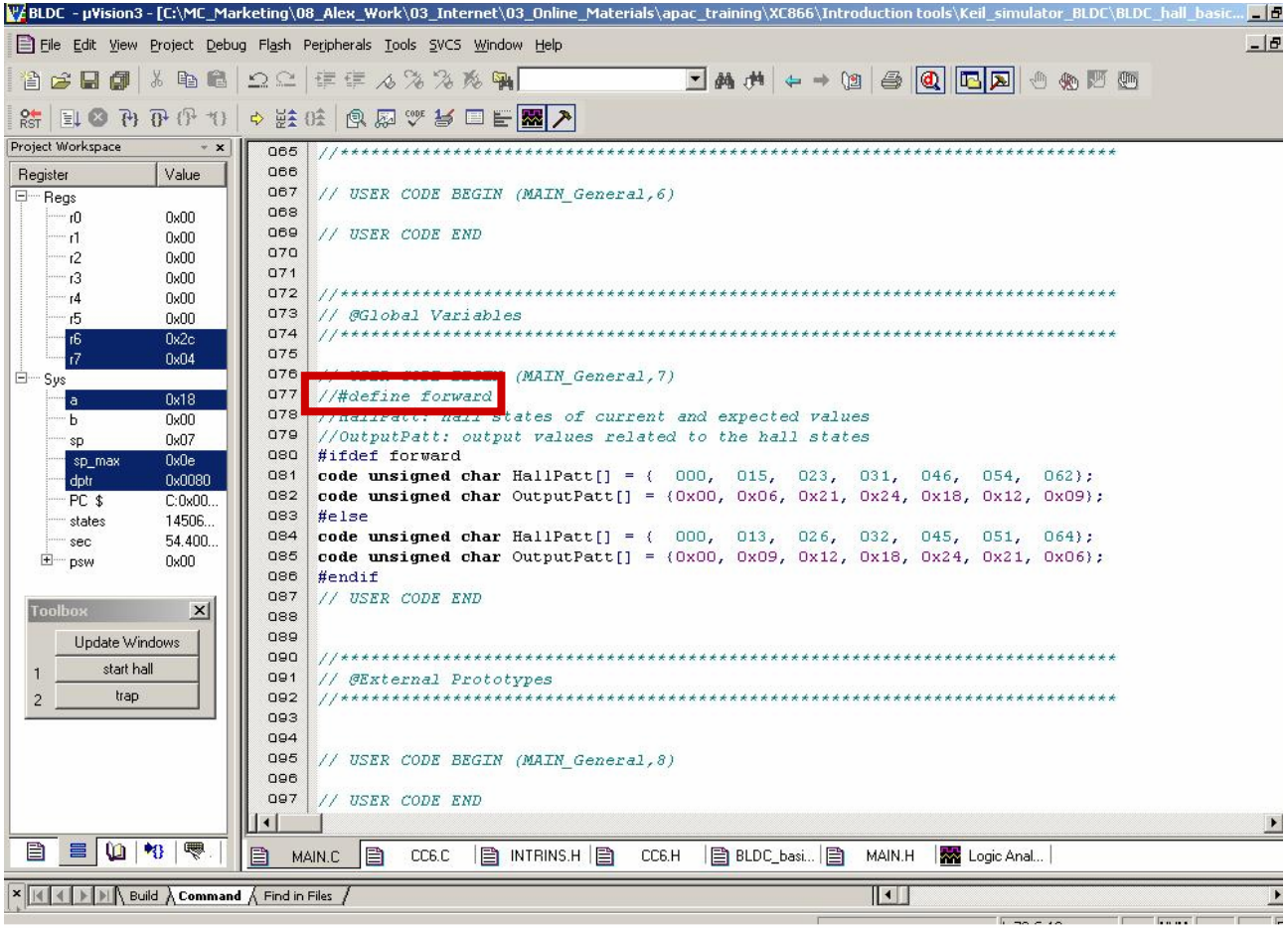


Compile and run Debug session with Logic Analyzer

- Change the direction by commenting out the 'forward'. Compile and execute again



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